

Fabrication and characterization at high temperature of AlGaN/GaN enhancement-mode HEMTs

S. Martín-Horcajo*, M. J. Tadjer, M. F. Romero, R. Cuervo, F. Calle

Dpto. de Ingeniería Electrónica and Instituto de Sistemas Optoelectrónicos y Microtecnología
ETSI Telecomunicación, Universidad Politécnica de Madrid
Av. Complutense 30, 28040 Madrid, Spain.

(*)E-mail: smartin@die.upm.es

Abstract—Enhancement-mode (E-mode) high electron mobility transistors (HEMTs) based on a standard AlGaN/GaN heterostructure have been fabricated using two different methods: ^{19}F implantation and fluorine-based plasma treatment. The need of a thermal annealing after both treatments has been proven in order to restore the I_D and g_m levels. DC characterization at high temperature has demonstrated that I_D and g_m decrease reversibly due to the reduction of the electron mobility and the drift velocity. Pulsed measurements (state period and variable pulse width) have been performed to study the self-heating effects.

Keywords— HEMT; enhancement-mode; transconductance; drain current; implantation; plasma treatment; annealing

I. INTRODUCTION

High electron mobility transistors (HEMTs) based on GaN are suitable for the development of high power switches, microwave amplifiers and high temperature integrated circuits (ICs), thanks to their excellent physical properties such as high electron saturation velocity, high electric breakdown field and good thermal conductivity [1, 2]. Enhancement-mode (E-mode) devices, with a zero or positive threshold voltage (V_{TH}), are more desirable than conventional depletion-mode (D-mode) devices in those applications because they provide the advantages of a simpler circuit design and fail-safe operation. Different approaches have been reported to fabricate E-mode devices starting from as-grown D-mode HEMT structures, including ^{19}F implantation [1], gate recess [3] and/or fluorine-based plasma treatment of the region under the gate [4, 5]. Most of their applications involved the performance at high temperature, either due to the environment or generated by the device operation (self-heating). Therefore, the study of thermal related issues is essential for the optimization of E-mode HEMTs.

In this paper, we have fabricated E-mode AlGaN/GaN HEMTs from a standard D-mode heterostructure using two different methods: ^{19}F implantation and fluorine-based plasma treatment; as well as we have carried out the study of their DC performance at high temperature and the evaluation of the self-heating effects using pulsed measurements.

II. DEVICE STRUCTURE AND FABRICATION

The HEMT structure consisted of 2 nm GaN/21.6 nm $\text{Al}_{0.28}\text{Ga}_{0.72}\text{N}$ /1 μm GaN/330 μm Si, grown by MBE. The process flow is illustrated in Fig. 1.

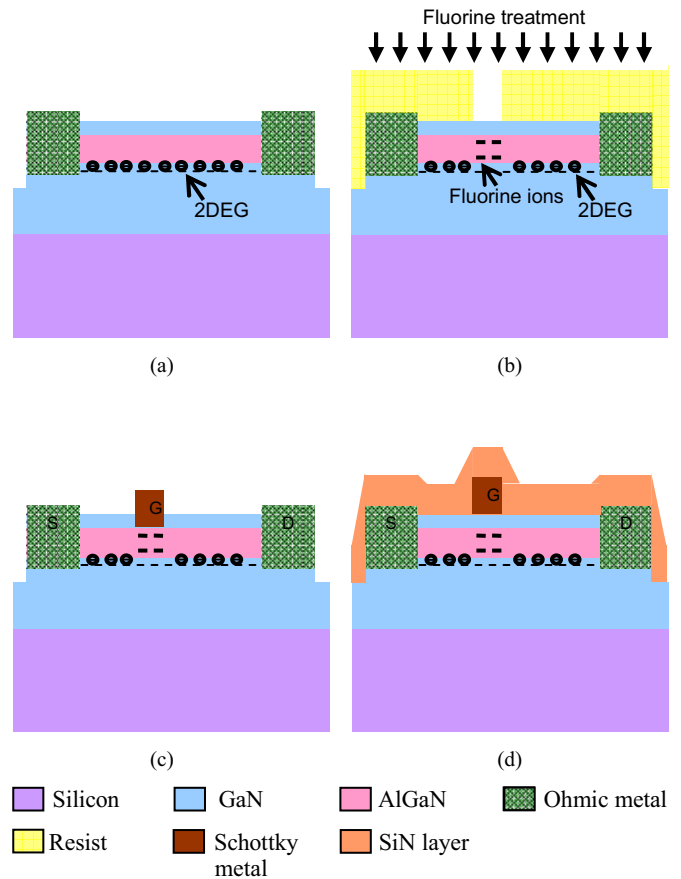


Figure 1. Schematics of the process flow of both fabrication methods of E-mode HEMTs: (a) mesa and ohmic metal; (b) gate area definition and F-treatment (^{19}F implantation or fluorine-based plasma); (c) Schottky metal, and (d) passivation through a SiN layer deposition.

At first, a 20/120/40/50 nm thick Ti/Al/Ni/Au multilayer was deposited for ohmic contacts and annealed at 870°C during 30 s in flowing N₂ atmosphere, followed by electrical contact isolation using Ar/SF₆-based plasma reactive ion etching (RIE) (Fig. 1a). E-beam lithography was used to define the gate length. The length and width gates were 0.7 μm and 2x50 μm, respectively (Fig. 2). Subsequently, the gate area was treated either by ¹⁹F implantation (50 KeV energy, 5·10¹² cm⁻² dose) or CF₄ plasma, (60 W power, 220 V DC bias, 33 mTorr pressure, 26% gas flow rate, 200 s) to achieve normally off operation likely due to the introduction of negative charged ions underneath the gate, therefore depleting the 2D electron gas (Fig. 1b). The gate electrode was formed by e-beam evaporation of Ni/Au (30/170 nm) and lift-off (Fig. 1c). Finally, the devices were passivated with a Si₃N₄ layer deposited by plasma-enhanced CVD (Fig. 1d).

After gate electrode formation, a thermal annealing was done at 400°C for 9 min in flowing 5% H₂/N₂ atmosphere to recover some of the damage caused by the prior fluorine treatment. In this way, a significant portion of the drain current (I_D) and the transconductance (g_m) levels were restored (Fig. 3).

Control samples of D-mode HEMTs were fabricated by omitting the F treatment under the gate and ulterior annealing in the process described above.

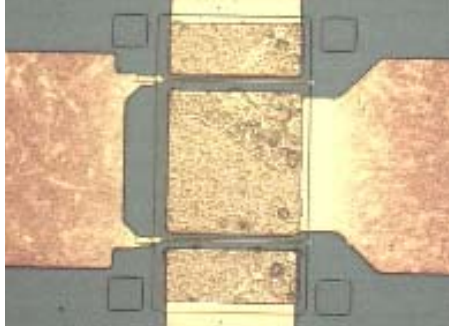


Figure 2. Optical image of an E-mode HEMT fabricated during this work.

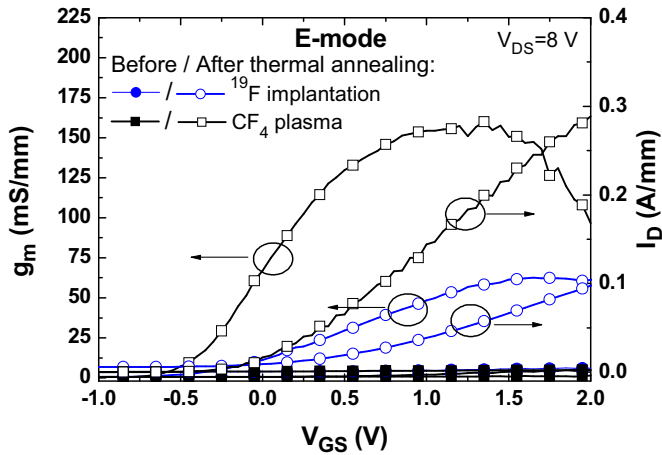


Figure 3. Recovery of I_D and g_m after thermal annealing. Solid symbols are related to before annealing and empty symbols correspond to after annealing.

III. EXPERIMENTAL DETAILS

The DC performance at high temperature of E-mode HEMTs is relevant for their application in high temperature power switching applications, as well as an aging test for reliability. DC measurements of I_D and g_m at different temperatures, from room temperature (RT) to 500 K with a step of 50 K, have been carried out using an Agilent 4156C semiconductor parameter analyzer and a Wenesco hot plate.

On the other hand, the drain high voltage and current required in such circuits causes self-heating effects, the importance of which can be evaluated by means of a combined DC/pulsed measurement technique that we have previously reported [7]. DC and V_{DS} pulsed measurements have been carried out at high temperature, from 300 K to 500 K with a step of 100 K, to evaluate possible self-heating effects by means of a method utilizing a PC-controlled Agilent A33250 function generator (pulsed V_{DS}, 100 μs period, 0.6-100% duty cycle), and Agilent E3647A DC voltage source for gate bias, a Yokogawa DL1720 digital oscilloscope, and a Wenesco hot plate.

IV. RESULTS AND DISCUSSION

Fig. 4 shows the transfer characteristics of HEMT devices processed by CF₄ plasma, ¹⁹F implantation, and the D-mode reference. From the g_m versus V_{GS} curve, a threshold voltage (V_{TH}) of -3.5 V was obtained for D-mode HEMTs, whereas it was around -0.45 V and -0.35 V for devices fabricated by fluorine-based plasma and ¹⁹F implantation, respectively. This difference of about 3 V in V_{TH} allows us to consider that F-treated HEMTs exhibit E-mode operation. DC characterization at RT revealed that E-mode HEMTs fabricated using the fluorine-based plasma treatment showed similar I_D and g_m levels than D-mode devices. However, devices fabricated using ¹⁹F implantation presented lower I_D and g_m. This can be explained because the implantation energy was high enough to incorporate F ions into the channel and/or affect its crystal structure, which can significantly reduce the channel electron mobility as well as the transconductance of the devices [1].

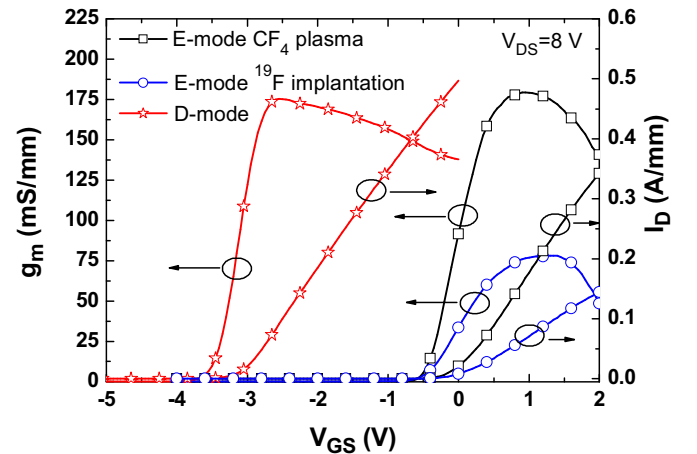


Figure 4. Transfer characteristics of a D-mode HEMT and two E-mode HEMTs fabricated using for one fluorine-based plasma treatment and ¹⁹F implantation for the other. V_{TH} was calculated as the intercept of the maximum g_m curve with the V_{GS} axis.

DC characterization at high temperature showed an almost linear decrease of I_D and g_m parameters for E-mode devices fabricated using both methods (see Figs. 5 and 6, respectively). This dependence was similarly observed in D-mode devices [6], where it was attributed to the reduction of the electron mobility and the drift velocity. These thermal effects on I_D and g_m values are reversible, as are also shown in Fig. 5 and Fig. 6.

In devices fabricated using ^{19}F implantation, the implantation damage to the channel had reduced I_D and g_m to a greater extent (Fig. 4). As a consequence, the temperature dependence of those parameters was weaker which means a lower reduction of the I_D and g_m comparing with the other devices (see Table. 1).

TABLE I. REDUCTION OF $I_{D,\text{max}}$ AND $g_{m,\text{max}}$ WITH THE TEMPERATURE.

Reduction of % of initial value	Reference	CF_4 plasma	^{19}F implantation
$I_{D,\text{max}}$	35	10	6
$g_{m,\text{max}}$	27	25	6

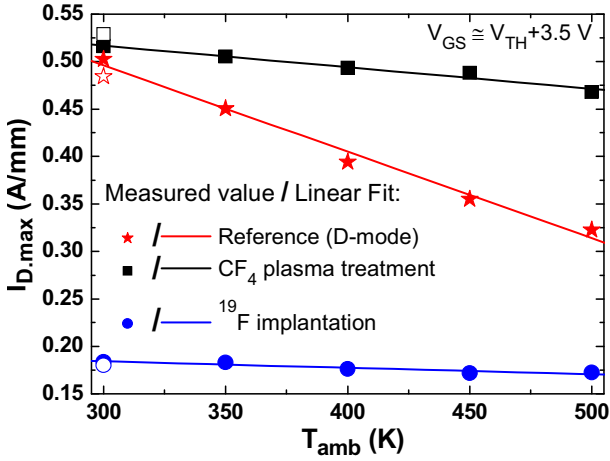


Figure 5. I_D dependence on the temperature. Solid symbols are related to before annealing and empty symbols correspond to after annealing.

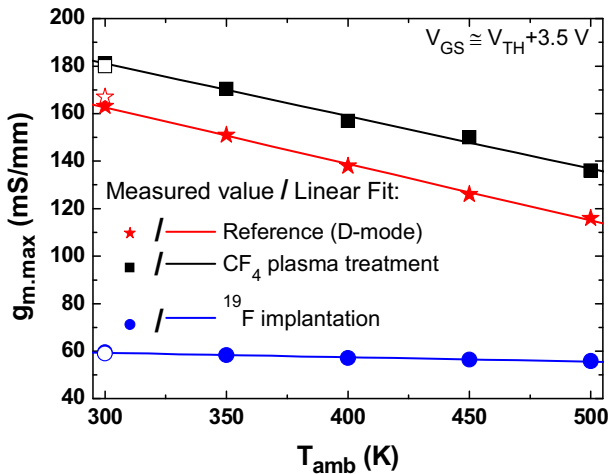


Figure 6. g_m dependence on the temperature annealing. Solid symbols are related to before annealing and empty symbols correspond to after annealing.

Pulsed measurements have revealed self-heating effects which increase the total power loss in the device, as expected for devices on lower thermal conductivity substrates such as Si [7]. These effects have been proven to be less important for shorter duty cycles (see Fig 7). Lowest self-heating effects were observed in ^{19}F implantation devices because of their lower I_D level.

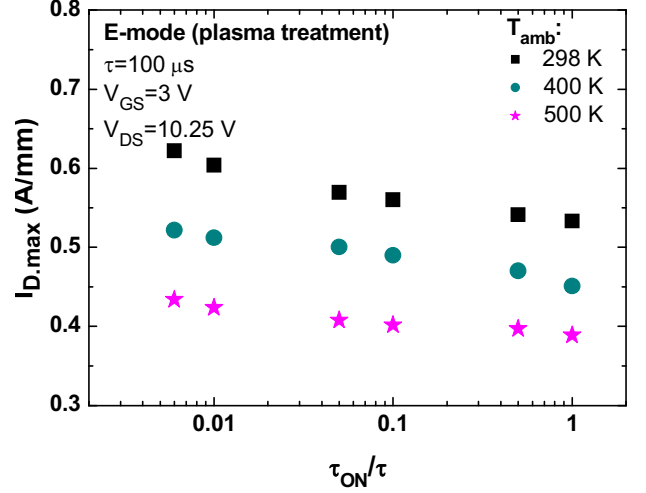


Figure 7. Self-heating effects as a function of pulse width on devices fabricated using fluorine-based plasma treatment.

The self-heating effects were reduced as temperature increases, as a consequence of the lower power dissipation due to the decrease of I_D (Fig. 7).

V. CONCLUSIONS

We have shown two different ways to fabricate E-mode HEMTs from a depletion mode AlGaIn/GaN structure. The fluorine plasma treatment allows to obtain E-mode devices with similar I_D and g_m levels to D-mode ones. DC measurements at high temperature have demonstrated the reversible dependence of I_D and g_m on the temperature. This dependence is weaker in devices fabricated by means of ^{19}F implantation due to the damages caused by this treatment. Variable pulse width current measurements reveal self-heating effects, which are lower at high temperature due to the reduction of I_D .

ACKNOWLEDGMENT

This work has been supported by the Spanish Ministerio de Ciencia e Innovación under the RUE (CSD2009-00046) and AEGaN (TEC2009-14307-C02-01) projects. The authors are grateful to Mr. David López-Romero and Ms. María del Carmen Sabido for technical assistance.

REFERENCES

- [1] Hongwei Chen, Maojun Wang, Kevin. J. Chen, "Enhancement-mode AlGaIn/GaN HEMTs fabricated by standard fluorine ion implantation", *Proceedings of CS ManTech Conference 2010*, Portland, OR, pp. 145-148.
- [2] Congwen Yi, Ruonan Wang, Wei Huang, Wilson C.-W. Tang, K. M. Lau, and Kevin J. Chen, "Reliability of enhancement-mode AlGaIn/GaN

HEMTs fabricated by fluorine plasma treatment”, *Proceedings of Electron Device Meeting 2007*, Washington, DC, pp. 389-392.

- [3] Yong Cai, Yugang Zhou, Kevin J. Chen, and Kei May Lau, “High-performance enhancement-mode AlGaIn/GaN HEMTs using fluoride-based plasma treatment”, *Electron Device Letters*, Vol. 26, No. 7, pp. 435-437, July 2005.
- [4] Wataru Saito, Yoshiharu Takada, Masahiko Kuraguchi, Kunio Tsuda, and Ichiro Omura, “Recessed-gate structure approach toward normally off high-voltage AlGaIn/GaN HEMT for power electronics applications”, *Transactions on Electron Devices*, Vol. 53, No. 2, pp. 356-362, February 2006.
- [5] T. Palacios, C.-S. Suh, A. Chakraborty, S. Keller, S. P. DenBaars, and U. K. Mishra, “High-performance E-mode AlGaIn/GaN HEMTs”, *Electron Device Letters*, Vol. 27, No. 6, pp. 428-430, June 2006.
- [6] R. Cuervo, F. Calle, A. F. Braña, Y. Cordier, M. Azize, N. Baron, S. Chenot, and E. Muñoz, “High temperature behaviour of GaN HEMT devices on Si(111) and sapphire substrates”, *Phys. Stat. Sol. (C)*, Vol. 5, pp. 1971-1973, April 2008.
- [7] S. Martin-Horcajo, R. Cuervo, E. Sillero and F. Calle, *34th European Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE)*, May 2010.